ADDRESSING SYSTEM FOR USE IN STORAGE DEVICES

FIELD OF THE INVENTION

The present invention relates to an auxiliary storage device and, in particular, to a high-capacity auxiliary memory unit constructed with a memory such as SDRAM and a SCSI (small computer system interface) bus structure.

BACKGROUND OF THE INVENTION

As personal computers are widely used, a client and server system based on the personal computers now can handle tasks that were once possibly executed by a main frame computer system. Typically, a client and server system includes a high-speed server with a large-capacity auxiliary memory unit and a plurality of personal computers (clients). The server and personal computers are connected via a network, thereby allowing the clients to access the server. Specifically, each client has the ability to write and read information to and from the server and to exchange information with other clients connected to the network.

However, an increased number of clients create a bottleneck between a server and auxiliary memory units. As a result, access time would be longer and, worst, due

to excessive load on the network, the network could be down or transmitted data could be lost.

In the client and server system, a hard disk drive (HDD) is dominantly used as an auxiliary memory unit. As is well known, the HDD is a large data storage device using magnetic disks. Data is stored to and read from a spinning disk by controllably positioning the read/write head over the disk. Thus, a reading/writing operation on the HDD requires a physical rotation of a motor and the lateral movement of the read/write head. In a server system such as game servers where tens of thousands of clients could simultaneously connect at one time, read and write requests from individual clients in the server can impose a serious load to the system. Servers with the HDD having a finite access time would not be able to handle ever increasing and faster data traffic. It could adversely affect the stabilization of the servers.

In a typical HDD, there is so-called access time, a time required to seek and change discs until a head is positioned over a sector. A drive motor is rotated to move the head over the sector where data is magnetically written and read. As is well known, while a high-performance SCSI bus provides a transmission rate of 320 Mega-bytes at the maximum, the HDD provides a transmission rate of 43 Mega-bytes at the maximum due to the aforementioned problems.

CPUs used in typical servers can address only upto

several Giga-byte memory map ranges so that they cannot directly control a data storage capacity over tens of Giga-bytes reaching several Tera-bytes. Furthermore, the CPUs fail directly to drive a plurality of memories due to a fan-out between memory chips.

SUMMARY OF THE INVENTION

It is, therefore, a primary objective of the present invention to provide a system, which is capable of dividing a memory into a plurality of equally-sized sub-memories and controlling an address of each sub-memory, thereby significantly increasing the access speed to an auxiliary memory unit.

In accordance with a preferred embodiment of the present invention, there is provided a system for addressing a data storage unit used in at least one of server and client computers, which comprises: means for converting an external bus into an internal bus for use in the system; a memory module for storing data on the internal bus therein, the memory module being divided into a plurality of equally-sized memory blocks; and means for processing writing data on the internal bus in the memory module and reading out the data therefrom.

BRIEF DESCRIPTIONS OF THE DRAWINGS

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 a schematic diagram of a memory addressing system in accordance with a preferred embodiment of the present invention;

Fig. 2 is a detailed block diagram of the PCI to memory controller shown in Fig. 1 in accordance with a preferred embodiment of the present invention;

Fig. 3 is a detailed block diagram of the PCI interface controlling unit shown in Fig. 2 in accordance with a preferred embodiment of the present invention; and

Fig. 4 is a schematic diagram of an expanded memory addressing system 200 in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In accordance with the present invention, a data seek time is removed by converting data position information in the HDD into a corresponding memory address so that a data access time is minimized to the order of several nano-seconds. Furthermore, the present

invention employs a PCI 66MHz/64bit bus to access internal memories, thereby supporting a transmission rate of 528Mbytes/second at maximum, which, in turn, meets the maximum transmission rate as mentioned above. As a result, Access speed to auxiliary memory unit is at least 12 times faster than that to the conventional HDD.

Referring to Fig. 1, there is shown a schematic diagram of a memory addressing system in accordance with a preferred embodiment of the present invention. The memory addressing system 100 comprises a SCSI interface controller 10, a memory card module 20, a CPU module 30, a PCI interface bus 40, and a control signal bus 50. The SCSI interface controller 10 converts an external SCSI (small computer system interface) bus into an internal PCI bus adapted to the memory addressing system 100, thereby allowing a SCSI bus command to be processed by the CPU module 30. As is well known, SCSI is one of the industry's standard interfaces that allows personal computers to communicate with peripheral devices, such as disk drives, tape drives, CD-ROM drives, printers, and scanners, faster and more flexibly than previous interfaces. SCSI ports are built into most personal computers today and supported by all major operating systems. SCSI is more flexible than earlier parallel data transfer interfaces.

The CPU module 30 controls all components of the SCSI interface controller 10, manages the internal PCI

bus, and converts a head, sector and cylinder representing position information of the HDD, and a track, sector and cluster representing format information of the HDD, which are inputted through the SCSI bus, into a corresponding memory address.

The memory card module 20, which is composed of SDRAM, Rambus DRAM, DDR or other equivalent memories, includes a memory controller 21 and a plurality of memory modules (e.g., 22) each of which has four equally-sized sub-memories.

The PCI interface bus 40 and the control signal bus 50 are internal local buses for processing internal data and control signals and use the standard PCI 64-bit bus interface.

In accordance with the present invention, the memory card module 20 is of a hierarchical configuration, which includes the PCI interface controlling unit and a multiplicity of sub-memories, to prevent the fan-out problem. The fan-out problem occurs when signals outputted from an original signal line are divided onto a number of lines for transmission, resulting in a decreased signal voltage. With the tree structure of the present invention, signals are compensated at an intermediate stage and forwarded to lower levels in the hierarchy, thereby eliminating signal loss problems. In a high-capacity memory, the division of signals from the original signal lines is increased so that signals to be

directed to each memory are eventually attenuated. Clock delay required for compensating the signals is in turn compensated by the memory controller 21.

Because the PCI to memory controller 21 employing a tree structure controls the memory module 22 distributed in a hierarchical fashion, it can drive a physical memory that is actually accessed while placing the rest of maintains in a low-power mode. As a result, power used to drive the memories is reduced and a back-up batter power can be extended.

Fig. 2 is a detailed block diagram of the PCI to memory controller shown in Fig. 1 in accordance with a preferred embodiment of the present invention.

As shown in Fig. 2, the PCI to memory controller 21 includes a first memory controlling unit 21a, a second memory controlling unit 21b and a PCI interface controlling unit 21c. The PCI interface controlling unit 21c processes a standard PCI command, control, data, which functions as a bridge between the PCI interface bus 40 and the first and second memory controlling units 21a and 21b. Each of the first and second memory controlling units 21a and 21b, responsive to a PCI command provided thereto from the PCI interface controlling unit 21c via a bus B2, performs a direct read/write operation for an internal memory to be accessed, and matches a cylinder, head, sector, information in the HDD to an address to process the data.

Specifically, the first memory controlling unit 21a, responsive to the PCI command provided thereto from the PCI interface controlling unit 21c via the bus B2, performs a direct read/write operation for any sub-memory of the first memory module 22. The second memory controlling unit 21b, responsive to the PCI command provided thereto from the PCI interface controlling unit 21c via the bus B2, performs a direct read/write operation for any sub-memory of the second memory module 23. On the other side, both of the first and second memory controlling units 21a and 21b process a high-capacity memory so that the activation of the overall memory requires a considerable amount of power consumption. As such, during the read/write operation of the memory, the first memory controlling unit 21a or the second memory controlling unit 21b activate only a memory corresponding to an address provided thereto from the PCI interface controlling unit 21c and maintains the remaining in a low power mode. As a result, the power consumption may be minimized.

Fig. 3 is a detailed block diagram of the PCI interface controlling unit shown in Fig. 2 in accordance with a preferred embodiment of the present invention. A detailed description of the internal operation algorithm of the PCI interface controlling unit 21c will be given with reference to Fig. 3.

As shown in Fig. 3, the PCI interface controlling

unit 21c includes a configuration (CFG) register R/W 1, an I/O write 2, a memory R/W 3, and a register block 7 having a lower address bit 4, an upper address bit 5 and a select bit 6. Note that, during the design of the PCI interface controlling unit 21c, from the perspective of a memory map of CPU regardless of a general-purpose or single-purpose system, the presence of an address region, which allows the CPU to address and is separated from the operation of the system, is basically required.

The lower address bit 4 of the register block 7 represents an address of a set region within the memory map, which is in the range of the address region. During the design of the memory controlling unit, the address range to be PCI interfaced is determined, and a bit range in which the lower address bit 4 is used is set, so that the lower address bit 4 is available.

The upper address bit 5 is set when a memory address region from which the memory map provided by the CPU is departed. In the upper memory address region, it is necessary to previously set a bit range based on a capacity range to be used during the design of the PCI interface controlling unit 21c.

The select bit 6 is used to directly access the memory modules and handle the fan-out to be occurred during the application of a single activation, thereby resulting in an increased expansion. From at least one bit to the maximum of the lower address region should be

assigned to the select bit 6.

A description of the operation algorithm of the PCI interface controlling unit will be given.

During the design of the PCI interface controlling unit 21c, the lower address bit 4, the upper address bit 5 and the select bit 6 are set based on a predetermined value. The I/O write 2 sets the upper address bit 5 on the register prior to the access to the memory using a PCI memory read/write command among the PCI commands. During the memory access, the lower address bit is accessed and the lower bit is concatenated with an upper bit of the register which is used at the I/O interface. Thus, the sum of the upper address bit and the lower address bit is used as an access memory address bit. The most significant bit of the register is used to select any of the memory modules.

Specifically, in a CPU system with 32-bits address region for example, provided that the PCI interface controlling unit 21c is designed in conditions that from the perspective of the CPU the lower address bit is set to be 19-bits, the memory map region is set to be 1Mbytes, the upper address bit to be I/O read and written is set to be 11-bits (i.e., 2048 bytes), and the select bit is set to be 2-bits, an available capacity of the PCI interface controlling unit may be calculated as 32 Gbytes as follows:

((1Mbytes*2Kbytes)*4bytes)*4bytes = 32Gbytes

In this manner, the application of the lower address bit, the upper address bit and the select bit to the 32-bits address region results in the capacity of 1,280,000 Tbytes. Similarly, the application of them to 64-bits, 128-bits, 512-bits address region and the like results in an astronomical capacity. Accordingly, although a change in the system and requirements of the capacity increase in geometric progression, the present invention has the ability to easily address the change and the requirements.

Fig. 4 is a schematic diagram of an expanded memory addressing system 200 in accordance with another embodiment of the present invention.

As shown in Fig. 4, a plurality of PCI bridges 110, 120, ... is used to expand the system while minimizing a change in hardware, each of the PCI bridges being provided between the PCI buses. In accordance with the present invention, although the SCSI interface controller is used based on Ultra-160 SCSI scheme for a data transmission between an external interface via the PCI bus, another data bus transmission scheme such as an IDE (Integrated Device Electronics), ATA (Advanced Technology Attachment), IEEE (Institute of Electrical and Electronics Engineers) 1394 may be used in lieu of the SCSI.

As demonstrated above, the present invention employing a tree hierarchical configuration,

automatically activates individual SDRAM control blocks, which are not accessed in a low power mode, which, in turn, results in minimized power consumption and a low power activation.

Furthermore, in accordance with the present invention, the application of a lower address bit, an upper address bit and a select bit to various types of address regions results in an astronomical capacity, which may be controlled by CPU. Thus, although a change in the system and requirements of the capacity increase in geometric progression, it has the ability to easily address the change and the requirements.

While the present invention has been described and illustrated with respect to a preferred embodiment of the invention, it will be apparent to those skilled in the art that variations and modifications are possible without deviating from the broad principles and teachings of the present invention which should be limited solely by the scope of the claims appended hereto.